REMARKS

Favorable reconsideration of the present application is respectfully requested.

Claims 1-14 have been amended to improve grammar and address various informalities. Without acceding to the rejections under 35 U.S.C. §§ 102 and 103, Claims 1, 4, 8 and 10 have been amended to more clearly recite certain distinctive features of the invention. Applicants respectfully submit that the rejections under §§ 102 and 103 are inappropriate, at least insofar as considered visavis the claims as now presented.

Claim 1 is directed to a microprocessor and recites, inter alia, a first clock terminal, coupled to a clock generating circuit, to supply a first clock signal to a first external device, and a second clock terminal, coupled to the clock generating circuit, to supply a second clock signal to a second external device, in parallel with said first clock signal, the second clock signal having a different frequency from said first clock signal. Kume (JP 405341872A), directed to a data processor, fails to teach or suggest these features.

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Moreover, none of the remaining references, taken either singly or in combination, teach or suggest these features.

Claim 4 is directed to a microprocessor and recites, inter alia, a frequency of a first clock signal is different from a frequency of a third clock signal, a frequency of a second clock signal is different from a frequency of a fourth clock signal and the first clock signal and the second clock signal are provided in parallel and external to the microprocessor. Kume fails to teach or suggest these features. Furthermore, Blomgren (USP 5,381,543), directed to a processor system with a dual clock, also fails to teach or suggest these features.

Moreover, none of the remaining references, taken either singly or in combination, teach or suggest these features.

Claim 8 is directed to a semiconductor module and recites, inter alia, a microprocessor chip including a clock pulse generator for generating a first clock signal, a second clock signal and a third clock signal. The second clock signal has a frequency lower from said first clock signal, the third clock signal has a frequency different from the first clock signal and different from the second clock signal, the clock pulse generator

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supplies, in parallel, the first and second clock signals external to the microprocessor chip, which is capable of accessing a memory chip synchronously with the first clock signal and an external device synchronously with the second clock signal. Kume fails to teach or suggest these features. Furthermore, Yanagiuchi (USP 5,684,418), directed to a clock signal generator, also fails to teach or suggest these features.

Moreover, none of the remaining references, taken either singly or in combination, teach or suggest these features.

Claim 10 is directed to a data processing system and recites, inter alia, a second pulse signal with a frequency lower than a first pulse signal, a first device operating in accordance with the first pulse signal applied through the first signal wire, a second device operating in accordance with the second pulse signal, a third device capable of controlling accesses to the first device in accordance with the first pulse signal and capable of controlling accesses to the second device in accordance with the second pulse signal, where the third device generates the first pulse signal, the second pulse signal and a third pulse signal. Kume fails to teach or suggest these features.

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Moreover, none of the remaining references, taken either singly or in combination, teach or suggest these features.

Accordingly, in view of the amendments presented herein, and for the reasons explained in the preceding remarks, Applicants submit that this application is in condition for allowance and should now be passed to issue.

A Notice of Allowance is respectfully solicited.

The Commissioner is hereby authorized to charge to Deposit Account No. 50-1165 any fees under 37 C.F.R. §§ 1.16 and 1.17 that may be required by this paper and to credit any overpayment to that Account.

If any extension of time is required in connection with the filing of this paper and has not been requested separately, then such extension is hereby requested.

Respectfully submitted,

July 26, 2004

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